imm 8-82 CENTRAL PROCESSOR MODULE

- **Complete Central Processor Module with system clocks, interface and control for memory, I/O ports, and real time interrupt**
- **The heart of this module is Intel's 8008-1 processor on a chip — p-channel silicon gate MOS**
- **48 instructions, data oriented**
- **Accumulator and six working registers**
- **Direct addressing of up to 16,384 bytes of memory. (PROM, ROM, or RAM)**
- **Directly addresses eight input ports and twenty-four output ports**
- **Subroutine nesting to seven levels**
- **Real time interrupt capability**
- **Direct memory access capability**
- **Interface to memory, I/O and interrupt ports through separate TTL buses**
- **Two phase crystal clock — 800kHz**
- **12.5μs instruction cycle**

The imm8-82 Central Processor Module is a complete 8-bit parallel central processor unit. It contains complete control for interface to memory and I/O. This is the main module in Intel's Intellec™ 8 systems.

The imm8-82 is built around Intel's 8008-1 CPU on a chip. It executes 48 instructions including conditional branching, register to register transfers, arithmetic, logical and I/O instructions. Six 8-bit registers and an 8-bit accumulator are provided. Subroutines may be nested to seven levels. Real time interrupt capability is provided and the processor may directly address up to 16,384 bytes of memory.

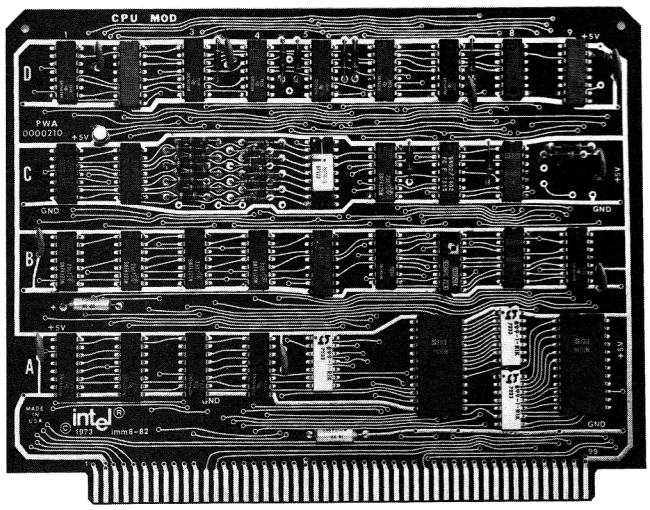
The imm8-82 has a fourteen bit TTL compatible memory address bus, an 8-bit data output bus and an 8-bit memory data input bus. Memory read and write signals and the wait request signal provide interface at TTL levels to any type of memory (including PROM, ROM, and RAM). Asynchronous interface to slower speed memories (access $> 1\mu s$) is provided by the wait request signal. This causes the processor to wait for memory response to a read or write command.

The Central Processor Module directly addresses up to eight 8-bit input ports and twenty-four 8-bit output ports. The 5-bit I/O address is contained in the upper byte of the memory address bus. Addresses 0 through 7 are defined as input ports, and 8 through 31 as output ports. Control signals, I/O cycle, I/O in and I/O out, define the I/O cycle and its function. An 8-bit data output bus and an 8-bit data input bus, both TTL compatible, provide data channels in and out of the processor module.

Real time interrupt capability and direct memory access capability complete the list of functional features for the imm8-82. During an interrupt, the Central Processor Module responds to the instruction presented at the 8-bit interrupt instruction port. Unless the main program flow is altered by the interrupt instruction, the execution will continue where it left off before processing the interrupt. Eight bits of data including sign, carry, zero and parity flags are latched on a separate bus during the execution portion of most instructions.

The direct memory access capability allows an alternate source to access memory or I/O while temporarily suspending processor operation. At the end of this alternative access to memory, the processor may return to normal program execution.

All system timing is derived from a two phase crystal clock running at 800kHz. This gives a machine cycle time of 12.5$\mu s \pm 0.01\%$ and provides an accurate timing source for software delay loops and other timing requirements.



Central Processor Module

Central Processor Module Specifications

Word Size:	Instruction: 8, 16, or 24 bits Data: 8 bits
Central Processor:	8008-1 CPU, 8 bit accumulator, six 8-bit registers, subroutine nesting to seven levels, interrupt capability, asynchronous operation with memory
Instruction Set:	48 including conditional branching, binary arithmetic, logical operations, register-to-register transfers, and I/O
Memory Addressing:	Any combination of PROM, ROM and RAM up to 16,384 bytes
Memory Interface:	Address: 14 bits TTL latching bus Data: 8-bit TTL bus to and from memory
I/O Addressing:	Input: Eight 8-bit input ports Output: twenty-four 8-bit latching output ports
I/O Interface:	8-bit TTL compatible buses to and from CPU. 8-bit TTL latched bus with execution data including flags (sign, parity, zero, and carry information)
System Clock:	Crystal controlled, 800kHz ± 0.01% Processor cycle time: 12.5μs
Connector:	Dual 50-pin on 0.125 in. centers. Connectors in rack must be positioned on 0.5 in. centers min. Wirewrap P/N C800100 from SAE P/N VPB01C50E00A1 from CDC
Board Dimensions:	6.18 in. x 8.0 in. x 0.062 in. Board to be on 0.5 in. centers minimum
Operating Temp:	0°C to +55°C
DC Power Requirements:	V_{CC} = +5V ± 5%, I_{CC} = 2.2A max, 1.0A typical V_{DD} = −9V ± 5%, I_{DD} = 0.06A max., 0.03A typical
Support Software:	PL/M Compiler Cross Assembler Simulator Written in FORTRAN IV

imm8-82 Block Diagram